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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device testing device which uses when examining the semiconductor device which wrote in at high speed and equipped the memory which can be read, and operates using a suitable semiconductor device test method and this test method.

[0002]

[Description of the Prior Art] Into the form of the memory which consists of semi-conductors, data are inputted with a clock, data are written in a semiconductor device synchronizing with a clock, the data which synchronized with the clock with the clock are outputted from a semiconductor device, and the memory which delivers data using the timing of this clock exists. The situation at the time of read-out of this kind of memory is shown in drawing 10. DA and DB which are shown in drawing 10 A, and DC-- show the data (data outputted from one certain pin) outputted from a semiconductor device. TD1 and TD2 -- show each test cycle. DQS shown in drawing 10 B shows the clock outputted from memory. Data DA and DB and DC-- are outputted from a semiconductor device synchronizing with this clock DQS. This clock is used in the condition of using, as a synchronizing signal at the time of delivering Data DA and DB and DC-- to other circuits (data strobe).

[0003] The time difference (phase contrast) dI1 and dI2 from the standup of each clock DQS (this clock is called a reference clock below) and the timing of falling to the changing point of data and the item which measures dI3 -- are in one of the trial items in the case of examining this kind of semiconductor device. These time difference dI1, dI2, and dI3 -- For example, as much as possible, it is evaluated as a device in which a response has the quickly excellent property, so that it is short. The grade of an examined semiconductor device is determined by the merits and demerits of this time difference.

[0004] In the condition that the reference clock DQS outputted from an examined semiconductor device is used, the clock generated in the source of a clock is impressed to a semiconductor device, this clock is supplied to the circuit inside a semiconductor device, and data are outputted synchronizing with this clock. Therefore, also when examining with a testing device, a clock is impressed to an examined semiconductor device from a testing-device side, and the clock passes along the interior of an examined semiconductor device, and is outputted as a reference clock for data delivery with data. Therefore, the standup of this reference clock and the timing of falling are measured, and they are these measured data DA, DB, and DC from the timing of a standup and falling. -- The time amount dI1 and dI2 to a changing point and dI3 -- will be measured.

[0005] Since the reference clock outputted from a semiconductor device as mentioned above passes through the interior of the semiconductor device and is outputted, the timing of the standup and the timing of falling receive greatly external environmental influence, such as the interior of each semiconductor device, and temperature, and as shown in drawing 11, the phenomenon of reference clocks DQS1 and DQS2 and DQS3 -- which a difference generates in a phase is seen for every semiconductor device. what furthermore depends the difference of a phase on the difference in each semiconductor device -- in addition, the phenomenon which the so-called jitter J changed according to the difference in the address of the memory accessed also inside a semiconductor device and the passage of time (thermal change) generates is also seen.

[0006] Therefore, from the timing of the standup of a reference clock DQS, and the timing of falling, in order [of Data DA and DB and DC--] to measure the time amount dI1 and dI2 to a changing point, and dI3 -- to accuracy, the timing of the standup of the reference clock DQS first outputted from a semiconductor device and the timing of falling must be measured to accuracy. For this reason, conventionally, the impression timing of the strobe pulse of the signal reading circuit with which the semiconductor device testing device is equipped was moved gradually, the

standup of a reference clock DQS and the timing of falling were measured, and time amount dI1 and dI2 and dI3 -- are measured using that measurement result.

[0007] The configuration of the part for measuring the standup of the reference clock DQS conventionally used for drawing 12 and the timing of falling is shown. A level comparator 10 is constituted by the electrical-potential-difference comparators CP1 and CP2 of a couple, and it judges whether the logical value of the reference clock DQS which examined semiconductor device DUT outputs by the electrical-potential-difference comparators CP1 and CP2 of these couples fulfills the electrical-potential-difference conditions of normal. The electrical-potential-difference comparator CP 1 judges whether the electrical-potential-difference value of H logic of a reference clock DQS is beyond the electrical-potential-difference value VOH of normal. Moreover, the electrical-potential-difference comparator CP 2 judges whether the electrical-potential-difference value by the side of L logic of a reference clock DQS is below the electrical potential difference VOL of normal.

[0008] These judgment results are inputted into the signal reading circuit 11, and the timing of the standup of a reference clock DQS and the timing of falling are measured in this signal reading circuit 11. The signal reading circuit 11 performs actuation which reads the logical value then inputted for every impression timing of a strobe pulse STB. For every test cycle, little by little, phase contrast (τT) is given and a strobe pulse STB is impressed. That is, actuation which a strobe pulse STB is given at a time to one signal reading circuit 11 for every test cycle, and reads the condition of the output of the electrical-potential-difference comparators CP1 and CP2 is performed.

[0009] A logic comparator 12 compares the expected value (the example of drawing H logic) beforehand determined as the logical value which the signal reading circuit 11 outputs, and when the logical value which the signal reading circuit 11 outputs is in agreement with expected value, it outputs the pass signal PA showing pass (good). Time amount T1 is got to know from the generating timing (the generating timing of a strobe pulse STB is known) of the strobe pulse STB 1 which read that the output of a level comparator 10 was reversed in H logic, and the timing of the standup of a reference clock DQS is determined.

[0010] When detecting the timing of falling of a reference clock DQS, generating of a strobe pulse STB determines the timing of falling by the strobe pulse which read the condition that started and the output of the electrical-potential-difference comparator CP 2 reversed generating in H logic like the detection which starts to the timing after the timing which started in H logic of a reference clock DQS.

[0011]
[Problem(s) to be Solved by the Invention] Since the generating timing of a reference clock DQS is conventionally measured using the timing measurement means using the strobe pulse STB impressed to the signal reading circuit 11 with which the semi-conductor testing device is equipped, and this signal reading circuit 11 as mentioned above, in order that what cycle may also repeat measuring the standup of a reference clock DQS, and the timing of falling and it may perform a test cycle TD, there is a fault which requires time amount.

[0012] And since measurement of the standup of a reference clock DQS and the timing of falling must be measured over all from initiation of a test pattern to termination when avoiding the effect of the jitter by all addresses or generation of heat that should be examined, long time amount is needed for measuring the standup of a reference clock, and the timing of falling. Although taking coarsely phase contrast τT which gives the time amount which measures the standup of a reference clock DQS and the timing of falling to a strobe pulse STB as an approach of shortening, and reducing the count of activation of a test cycle is also considered If phase contrast τT given to a strobe pulse STB is changed coarsely, the standup of a reference clock DQS and the timing measuring accuracy of falling will fall. As this result, they are a reference clock DQS and Data DA, DB, and DC. -- There are the time amount dI1 and dI2 to a changing point and a fault of dI3 -- to which the dependability of a measurement result falls.

[0013] Moreover, the object of this invention tends to offer extremely the semiconductor device testing device using the semiconductor device test method which can measure the standup of a reference clock, and the timing of falling with a sufficient precision, and this test method for a short time.

[0014]
[Means for Solving the Problem] The reference clock with which carrier delivery of this data is presented in claim 1 of this invention along with the data outputted from an examined device is outputted. In the semiconductor device testing device by which the timing of this reference clock and the time amount to the changing point of data are measured, and an examined device is evaluated according to the measurement value of this time amount While measuring and memorizing the timing to which a reference clock is beforehand outputted for every test cycle over all the examined addresses The semiconductor device test method which determines the measurement result of each memorized test cycle as the criteria phase location for measuring the time amount to the changing point of data is

proposed.

[0015] In claim 2 of this invention, it sets to a semiconductor device test method according to claim 1. The polyphase pulse to which small [every] phase contrast was given one by one from the predetermined phase location of each test cycle for every test cycle is generated. By using this polyphase pulse as a strobe pulse of the signal reading circuit for detecting the generating timing of a reference clock The semiconductor device test method which measures the changing point of a reference clock by the phase number of the strobe pulse which detected the changing point of a reference clock is proposed.

[0016] In claim 3 of this invention, the phase number of the strobe pulse which detected the changing point of a reference clock in a semiconductor device test method according to claim 1 The memory possessing the address corresponding to the examined address of an examined semiconductor device memorizes. In case an examined semiconductor device is examined, a phase number is read from the address corresponding to the address impressed to the examined semiconductor device of memory, and the semiconductor device test method which determined the timing which reads the logical value of data by this read phase number is proposed.

[0017] In claim 4 of this invention, it sets to a semiconductor device test method according to claim 1. The phase number of the strobe pulse which detected the changing point of a reference clock is memorized by memory with the address corresponding to the address showing the chronological-order foreword of the test pattern impressed to an examined semiconductor device. A phase number is read from the address showing the chronological-order foreword of the test pattern impressed to the examined semiconductor device of memory in case an examined semiconductor device is examined. The semiconductor device test method which determined the timing which reads the logical value of data by this read phase number is proposed.

[0018] In claim 5 of this invention, in a semiconductor device test method according to claim 1, a strobe pulse is generated to the timing which matched with the phase number which detected the changing point of a reference clock, and was set up beforehand, and the semiconductor device test method which read the logical value of the data which an examined semiconductor device outputs by the timing of this strobe pulse is proposed. The data reading circuit which reads the logical value of the data which an examined semiconductor device outputs in claim 6 of this invention according to the impression timing of a strobe pulse, Two or more signal reading circuits prepared in order to measure the generating timing of the reference clock which an examined semiconductor device outputs, A polyphase pulse generating means to impress the strobe pulse which consists of polyphase pulses by which small [every] phase contrast was given to each of two or more of these signal reading circuits, Two or more comparison test means to compare with expected value the result which each of two or more signal reading circuits read, A conversion means to change the judgment result of two or more of these comparison test means into the phase number of the strobe pulse which detected the changing point of a reference clock, The memory which memorizes the phase number which this conversion means changed to the address corresponding to the address impressed to the examined semiconductor device, The timing selection circuitry which sets up the generating timing of the strobe pulse corresponding to this phase number whenever reading appearance of the phase number memorized by this memory is carried out, The semiconductor device testing device constituted as be alike is proposed as the strobe pulse generating circuit which generates the strobe pulse impressed to a data reading circuit according to the timing setting value set as this timing selection circuitry.

[0019] The data reading circuit which reads the data which an examined semiconductor device outputs in claim 7 of this invention according to the impression timing of a strobe pulse, Two or more signal reading circuits prepared in order to measure the generating timing of the reference clock which an examined semiconductor device outputs, A polyphase pulse generating means to impress the strobe pulse which consists of polyphase pulses by which small [every] phase contrast was given to each of two or more of these signal reading circuits, Two or more comparison test means to compare with expected value the result which each of two or more signal reading circuits read, A conversion means to change the judgment result of two or more of these comparison test means into the phase number of the strobe pulse which detected the changing point of a reference clock, The memory memorized to the address corresponding to the address showing the chronological-order foreword of a test pattern which impressed the phase number which this conversion means changed to the examined semiconductor device, The timing selection circuitry which sets up the generating timing of the strobe pulse corresponding to this phase number whenever reading appearance of the phase number memorized by this memory is carried out, The semiconductor device testing device constituted as be alike is proposed as the strobe generating circuit which generates the strobe pulse impressed to a data reading circuit according to the timing setting value set as this timing selection circuitry.

[0020] In claim 8 of this invention, it sets they to be [any of a semiconductor device testing device according to claim 6 or 7], and a polyphase pulse generating means is constituted by two or more delay elements from which a

time delay differs every only, and proposes the semiconductor device testing device made to generate the polyphase pulse to which the pulse was impressed to the delay element of these plurality, and small [every] phase contrast was given. In claim 9 of this invention, it sets they to be [any of a semiconductor device testing device according to claim 6 or 7], and a polyphase pulse generating means proposes the semiconductor device testing device which carried out cascade connection of two or more delay elements with the same time delay, and was considered as the configuration which acquires a polyphase pulse from each node of two or more of these delay elements that carried out cascade connection.

[0021] It sets in claim 10 of this invention they to be [any of a semiconductor device testing device according to claim 6 or 7]. Two or more comparison test means output the comparison test result to the comparison test means by which a time delay is long, next sequentially from a side with the short time delay of the strobe pulse which consists of polyphase pulses. Each comparison test means makes the judgment result to confirm output only from the comparison test means which detected the comparison test result and inequality of each preceding paragraph. The semiconductor device testing device considered as the configuration which changes the output bit position of this judgment result to confirm into the phase number of the strobe pulse which detected the changing point of a reference clock is proposed.

[0022]

[Function] According to the semiconductor device test method by this invention, since the standup of a reference clock and the timing of falling are measured using a polyphase pulse, the standup of a reference clock or the timing of falling can be measured within the time amount of 1 test cycle. And by taking small the phase contrast given to a polyphase pulse, the standup of a reference clock DQS and the timing accuracy of measurement of falling can be taken highly. Therefore, the standup of a reference clock and the timing of falling can be measured with a precision sufficient moreover for a short time, as this result, the measurement result to a changing point can be obtained in a short time, and the advantage of a reference clock DQS, Data DA and DB, and DC-- which can moreover improve dependability is acquired.

[0023]

[Embodiment of the Invention] Drawing 1 shows the configuration of the important section of the semiconductor device testing device which operates using the semiconductor device test method by this invention. Before explaining the important section of this invention shown in drawing 1, the outline of a testing device of using drawing 2 for a sense and examining a common semiconductor device is explained. The whole semiconductor device testing device is shown by the inside TES of drawing. The semiconductor device testing device TES is constituted by a master controller 13, a pattern generator 14 and a timing generator 15, the wave formatter 16, a logic comparator 12, a driver 17, the signal reading circuit 11, the failure-analysis memory 18, the source 19 of logic amplitude reference voltage, the source 21 of comparison reference voltage, and device power-source 22 grade. In addition, the level comparator 10 shown in drawing 12 here is shown as what is contained in the signal reading circuit 11.

[0024] Generally a master controller 13 is constituted by the computer system, and a pattern generator 14 and a timing generator 15 are mainly controlled according to the test program which the user created. Generate pattern generator 14 blank-test pattern data, and this test pattern data is changed into the test pattern signal which has a real wave by the wave formatter 16. It is impressed by examined semiconductor device DUT, and it is made to memorize through the driver 17 whose voltage is amplified to a wave with the amplitude value which set up this test pattern signal in the source 19 of logic amplitude reference voltage.

[0025] The reply signal read from examined semiconductor device DUT reads the logical value in the signal reading circuit 11. A logic comparator 12 judges with what has a defect in the memory cell of the read address when expected value and an inequality occur as compared with the expected value to which the logical value read in the signal reading circuit 11 is outputted from a pattern generator 14, the defect address is memorized in the failure-analysis memory 18 for every defect generating, and it judges whether relief of for example, a defect cel is possible at the test termination event.

[0026] Although drawing 2 shows the configuration of the testing device for one pin, actually, this configuration is prepared several pin minutes of examined semiconductor device DUT, and the input of a test pattern and incorporation of the reply signal of examined semiconductor device DUT are performed for every pin. As opposed to the pin PN which outputs a reference clock DQS as this invention shows to drawing 1 A level comparator 10, The polyphase pulse generator 30, and two or more signal reading circuits TC1, TC2, TC3, and TC4 and TC5 --, Two or more comparison test means PF1, PF2, PF3, PF4, and PF5--, These comparison test means PF1, PF2, PF3, PF4, and a conversion means 31 of PF5-- to change a judgment result into the phase number of a polyphase pulse, The timing

selection circuitry 33 which chooses and outputs the generating timing of a strobe pulse STB from the phase number read from memory 32 at the memory 32 which memorizes this phase number, and the time of a test, The semiconductor device testing device considered as the configuration which formed the strobe generating circuit 34 which generates a strobe pulse STB to the timing chosen by this timing selection circuitry 33 is proposed.

[0027] The polyphase pulse generator 30 shows the case where two or more delay elements DY1, DY2, DY3, and DY4 and DY5 -- which were set as the value from which a time delay differs every only constitute from this example. The polyphase pulse which has 100PS time difference in a time delay by [of each delay elements DY1, DY2, DY3, and DY4 and DY5 --] giving the time difference of every 100PS [for example,] (picosecond) can be generated. An example of a polyphase pulse is shown in drawing 3 B. From the predetermined phase location of a test cycle TD to the polyphase pulses P1, P2, P3, and P4 to which 100PS of phase contrast was given at a time -- Signal reading circuits TC1, TC2, TC3, TC4, and TC5 -- The input terminal of each strobe pulse is given.

[0028] Signal reading circuits TC1, TC2, TC3, TC4, and TC5 -- A level comparison result is inputted into each input terminal from a level comparator 10. Drawing 1 shows the configuration in the case of measuring the timing of the standup of a reference clock DQS. Therefore, the output of the electrical-potential-difference comparator CP 1 which performs the level comparison by the side of H logic to each input terminal of the signal reading circuits TC1, TC2, TC3, and TC4 and TC5 -- is inputted. Although the configuration which measures the timing by the side of falling of a reference clock DQS is omitted by drawing 1 , the configuration is the same as the configuration shown in drawing 1 , and is considered as the configuration which reads the output of the electrical-potential-difference comparator CP 2 which performs the level comparison by the side of L logic in that case by the polyphase pulse.

[0029] Signs that the timing of falling of a reference clock DQS is measured for signs that the timing of the standup of a reference clock DQS is measured to drawing 3 , to drawing 4 again are shown. Drawing 3 A and drawing 4 A show the wave of the reference clock DQS outputted from the pin PN which outputs the reference clock of examined semiconductor device DUT. The comparison electrical potential difference VOH is given to the electrical-potential-difference comparator CP 1 which constitutes a level comparator 10, and if the level of a reference clock DQS becomes higher than the comparison electrical potential difference VOH, the electrical-potential-difference comparator CP 1 will output H logic.

[0030] Therefore, if the strobe pulse which consists of polyphase pulses is impressed after the electrical-potential-difference comparator CP 1 outputs H logic, the signal reading circuit will output H logic. Comparison test means PF1, PF2, PF3, PF4, and PF5-- are expected value (this example H logic) and the signal reading circuits TC1, TC2, TC3, TC4, and TC5, respectively. -- Each reading result is compared and the signal reading circuits TC1, TC2, TC3, and TC4 and H logic of TC5 -- which expresses coincidence when an output and the expected value of H logic are in agreement are outputted.

[0031] Each comparison test means PF1, PF2, PF3, PF4, and PF5-- compare the judgment result and the signal reading result of self of a comparison test means of the preceding paragraph (comparison test means of a number with one young phase sequence foreword of a polyphase pulse) further, and after the inequality has occurred between the comparison test result of the preceding paragraph, and the signal reading result of self, they judge with it being effective, and they output the judgment result showing validity. The example of drawing 3 and drawing 4 shows the case where the judgment result of H logic as which comparison test means PF4 expresses validity is outputted.

[0032] An example of the concrete configuration of PF4 is shown in drawing 5 as an example of a comparison test means. Drawing 5 shows the case where it considers as the configuration which can be used also [circuit / which measures the timing of falling of a reference clock DQS]. therefore -- an electrical potential difference -- a comparator -- CP -- two -- an output side -- a signal -- reading -- a circuit -- TC -- four -- ' -- connecting -- a signal -- reading -- a circuit -- TC -- four -- TC -- four -- ' -- a strobe -- an input terminal -- **** -- drawing 3 -- and -- drawing 4 -- having been shown -- a polyphase -- a pulse -- P -- four -- and -- TC -- four -- ' -- a strobe pulse -- ***** -- giving -- having .

[0033] The inequality detection gate G4 which detects the inequality of OR gate G3 which takes the OR of the output of the gates G1 and G2 which measure expected value EXP and the output of the signal reading circuit TC 4 and TC4', and these gates G1 and G2, and the output of this OR gate G3 and the comparison test result of the preceding paragraph can constitute comparison test means PF4. The timing of the standup of a reference clock DQS is detectable on the system way which serves as the electrical-potential-difference comparator CP 1, the signal reading circuit TC 4 and the gate G1, and OR gate G3 from the inequality detection gate G4. H logic is given as expected value in the case of measuring the timing of the standup of a reference clock DQS, and L logic is set up as expected value in the case of detecting the timing of falling. By setting up the expected value of H logic, the gate G1

becomes effective and it supervises whether the output of the signal reading circuit TC 4 reverses this gate G1 in H logic.

[0034] If the output of the signal reading circuit TC 4 is reversed in H logic, the output of the gate G1 will also be reversed in H logic, and the H logic will be inputted into the inequality detection gate G4 through OR gate G3. An exclusive "or" circuit can constitute the inequality detection gate G4, and comparison test result P/F of the preceding paragraph is given to the input terminal of one of these. As for the inequality detection gate G4, not H logic but the reading result of the signal reading circuit TC 4 of self outputs H logic, only when comparison test result P/F of the preceding paragraph is reversed in H logic. The output of this H logic is supplied to PF5 the comparison test means of the next step, and here while it is inputted into the conversion means 31 shown in drawing 1 . In comparison test means PF5 of the next step, although the signal reading circuit PC 5 of self outputs H logic, since H logic is inputted from comparison test means PF4 of the preceding paragraph, the detection result of an inequality is not outputted but L logic is outputted.

[0035] Consequently, only a comparison test means by which the polyphase pulse was given to the beginning from the event of exceeding the comparison electrical potential difference V_{OH} prepared for the level comparison of the level of a reference clock DQS will output H logic. In addition, L logic is given to the inequality detection gate G4 of comparison test means PF1 of the first rank as a comparison test result of the preceding paragraph. If the signal reading circuit TC 1 of self outputs H logic by this, the inequality detecting signal of H logic will be outputted, and it detects that the reference clock DQS started in the early stages of a test cycle TD.

[0036] The conversion means 31 is each comparison test means PF1, PF2, PF3, PF4, and PF5. -- A comparison test result is incorporated and it changes into the data of the small number of bits as much as possible. That is, in this invention, it is characterized by the point considered as the configuration changed into the phase number of the polyphase pulse which gave comparison test means PF1, PF2, PF3, PF4, and the reading result of the signal reading circuit where each judgment result becomes effective of PF5-- . The conversion algorithm of the conversion means 31 is shown in drawing 6 . Although it is desirable to prepare only the number which can be set up at intervals of the strobe with which comparison test means PF1 and PF2 -- can be satisfied of the accuracy of measurement enough to the spec. of a device with the signal reading circuit TC 1 and TC2 --, it is shown as that in which eight comparison test means PF1 - PF8 exist here. When any one of eight comparison test means PF1 - the PF8 outputs H logic (1 shows by a diagram), that bit position is changed into numeric values 1-8, "1" is further subtracted from that numeric value, and the case where that subtraction result is changed into the numeric data D0-D7 of 4 bits in this example is shown. The numeric data D0-D7 of 4 bits can be dealt with as a number showing the phase sequence foreword of the polyphase pulses P1-P8. It can change into the number for 16 phases of 0-15 by 4 bits, and memory 32 is made to memorize this phase number.

[0037] By changing a 8-bit comparison test result into 4-bit phase number data in this way, the advantage which can make storage **** of memory 32 small is acquired. X and Y address which are impressed to examined semiconductor device DUT are changed into the suitable address (address suitable for the configuration of memory 32) from a pattern generator 14 in the address translation circuit 35 if needed, and the address impressed to examined semiconductor device DUT and the corresponding address are made to memorize each measured value in the example shown in drawing 1 . Therefore, memory 32 shall have equipped all the address spaces corresponding to the address, i.e., the examined address, which should examine examined semiconductor device DUT.

[0038] It precedes examining examined semiconductor device DUT, and writes in over all the examined addresses of an examined semiconductor device, read-out is performed, and the phase number of the polyphase pulse which measures for every address and is acquired as a result of the measurement which impressed the standup of the reference clock DQS outputted at the time of the read-out and the timing of falling to examined semiconductor device DUT is memorized in memory 32. In addition, measurement of the timing of falling of a reference clock DQS is the polyphase pulses P1, P2, P3, P4, and P5, as shown in drawing 4 . -- It is carried out by delaying a phase to the falling side of the constant-rate [every] reference clock DQS.

[0039] The standup of a reference clock DQS or the timing of falling is measured, and where the measurement result is incorporated in memory 32, the trial of examined semiconductor device DUT is started. The measurement result (phase number of a polyphase pulse) equivalent to the standup of the reference clock DQS outputted when the address was accessed from memory 32 in parallel with reading data from each address of examined semiconductor device DUT when examining examined semiconductor device DUT, or the timing of falling is read. The measurement result by which reading appearance was carried out is inputted into the timing selection circuitry 33 shown in drawing 1 , is this timing selection circuitry 33, and chooses the impression timing of the strobe pulse STB given to the signal reading circuit 11 for reading in examined semiconductor device DUT the data by which reading

appearance is carried out.

[0040] The outline of the timing selection circuitry 33 is shown in drawing 7. The timing selection circuitry 33 is constituted by selector 33B chosen according to the measurement result by which reading appearance is carried out [any of the generating timing memorized to timing memory 33A which memorized the generating timing of a strobe pulse STB, and this timing memory 33A they are, and] from memory 32. In timing memory 33A, they are 200PS, 300PS, 400PS, and 500PS. -- 16 kinds of time amount values are memorized. This time amount value is equivalent to the time amount value from the initial phase location of each test cycle TD, and is pointing to the standup of the measured reference clock DQS, or the timing of falling. The timing given with this time amount value serves as a criteria phase location which measures the time amount dI1 and dI2 to the changing point of the data which it is going to measure from now on, and dI3 --. This time amount value is chosen according to the measurement result incorporated in memory 32, and that selected time amount value is inputted into the strobe generating circuit 34.

[0041] The time amount (predetermined value) to the changing point of the data by which reading appearance is carried out to the time-amount value inputted from the timing selection circuitry 33 in the strobe generating circuit 34 from examined semiconductor device DUT adds or subtracts, a strobe pulse STB generates to the timing of that result of an operation, reading of data by which impresses this strobe pulse STB to the signal reading circuit 11, and reading appearance is carried out from examined semiconductor device DUT performs, and it examines whether the changing point of data exists to the timing of that strobe pulse.

[0042] That is, the architect of a semiconductor device grasps beforehand the time amount to the changing point of the data by which reading appearance is carried out from a semiconductor device from the standup of a reference clock DQS, or the timing of falling as a design value. Therefore, the standup of a reference clock DQS and the timing of falling are measured beforehand, and exact inspection can be carried out if it examines whether the changing point of data existed within the limits of the time amount planned from the standup of a reference clock DQS, and the timing of falling by making the timing into the known value.

[0043] Although **** explained the example which measures the standup of a reference clock DQS, or the timing of falling for every address of examined semiconductor device DUT, a semiconductor device can carry [the standup of a reference clock DQS, or the timing of falling] out the trial in consideration of the drift by heat by applying this invention also about the phenomenon changed gradually corresponding to the time amount (for example, drift by heat) from for example, initiation of operation.

[0044] Drawing 8 shows the example. The case where formed the cycle counter 36 which carries out counting of the number of cycles of the test pattern outputted from a pattern generator 14 in this example, carried out counting of what cycle eye of a test pattern is examined by this cycle counter 36, and it considers as the configuration which changes those enumerated data into the address signal of memory 32 in the address translation circuit 35, and accesses memory 32 by this address signal is shown. therefore, in advance of a trial, the standup of all the reference clocks DQS of a before [from initiation of a test pattern (test program) / termination] that carry out reading appearance and are outputted from semiconductor device DUT in the mode, or the timing location of falling is measured beforehand, and this measurement result is incorporated in memory 32. A trial is started in the condition of having measured over all until it ends the standup of a reference clock DQS, or the timing of falling from initiation of a test pattern. The standup of a reference clock DQS or the measurement result of the timing of falling is read from memory 32 during this trial. By determining the timing of the strobe pulse for reading the data by which reading appearance is carried out from an examined device using this measurement result Even if it changes the timing of a reference clock DQS gradually according to the passage of time, the timing which follows the fluctuation and reads data can also change, and the trial in consideration of the drift by heat can be carried out.

[0045] Drawing 9 shows the deformation example of the polyphase pulse generating means 30. This example shows the case where the delay elements DY1, DY2, DY3, and DY4 with few time delays and DY5 -- are considered as the configuration which generates the polyphase pulse to which cascade connection was carried out, and to which small [every] phase contrast was given from each of that node.

[0046]
[Effect of the Invention] the polyphase pulses P1, P2, P3, and P4 which were shown in drawing 3 and drawing 4 according to this invention as explained above, P5 --, and P1 -- ' -- P2', P3', P4', Since the standup of a reference clock DQS or the timing of falling is measured within the time amount of the 1 test cycle TD by using P5'--, as compared with the former, the standup of a reference clock DQS or the timing of falling can be measured extremely in a short time. as this result -- this kind of semiconductor device -- a short time -- and it can examine with a sufficient precision and the advantage which can heighten the employment effectiveness of a testing device is

acquired.

[0047] Moreover, since the standup of a reference clock DQS or the measurement result of the timing of falling was changed into the phase number of a polyphase pulse, the number of bits of data can be made small. Since storage capacity of memory 32 can be made small as this result, the increase of cost in the addition of this circuit can be made into the minimum.

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CLAIMS

[Claim(s)]

[Claim 1] The reference clock with which delivery of this data is presented along with the data outputted from an examined device is outputted. In the semiconductor device testing device by which the timing of this reference clock and the time amount to the changing point of the above-mentioned data are measured, and an examined device is evaluated according to the measurement value of this time amount While measuring and memorizing the timing to which the above-mentioned reference clock is beforehand outputted for every test cycle over all the examined addresses The semiconductor device test method characterized by determining the measurement result of each memorized test cycle as the criteria phase location for measuring the time amount to the changing point of the above-mentioned data.

[Claim 2] The semiconductor device test method characterized by measuring the changing point of the above-mentioned reference clock by the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock by generating the polyphase pulse to which small [every] phase contrast was given one by one from the predetermined phase location in a semiconductor device test method according to claim 1, and using this polyphase pulse as a strobe pulse of the signal reading circuit for detecting the generating timing of the above-mentioned reference clock.

[Claim 3] In a semiconductor device test method according to claim 1, the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock The memory possessing the address corresponding to the examined address of an examined semiconductor device memorizes. The above-mentioned phase number is read from the address corresponding to the address impressed to the examined semiconductor device of the above-mentioned memory in case an examined semiconductor device is examined. The semiconductor device test method characterized by determining the timing which reads the logical value of the above-mentioned data by this read phase number.

[Claim 4] In a semiconductor device test method according to claim 1, the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock is memorized by memory with the address corresponding to the address showing the chronological-order foreword of the test pattern impressed to an examined semiconductor device. The above-mentioned phase number is read from the address showing the chronological-order foreword of the test pattern impressed to the examined semiconductor device of the above-mentioned memory in case an examined semiconductor device is examined. The semiconductor device test method characterized by determining the timing which reads the logical value of the above-mentioned data by this read phase number.

[Claim 5] The semiconductor device test method characterized by reading the logical value of the data which are made to generate a strobe pulse to the timing which matched with the phase number which detected the changing point of the above-mentioned reference clock in the semiconductor device test method according to claim 1, and was set up beforehand, and an examined semiconductor device outputs by the timing of this strobe pulse.

[Claim 6] A and the data reading circuit which reads the logical value of the data which an examined semiconductor device outputs according to the impression timing of a strobe pulse, Two or more signal reading circuits prepared in order to measure the generating timing of the reference clock which B and the above-mentioned examined semiconductor device output, C and a polyphase pulse generating means to impress the strobe pulse which consists of polyphase pulses by which small [every] phase contrast was given to each of two or more of these signal reading circuits, Two or more comparison test means to compare with expected value the result which each of D and two or more above-mentioned signal reading circuits read, E and a conversion means to change the judgment result of two or more of these comparison test means into the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock, The memory which memorizes the phase number which F and this conversion means changed to the address corresponding to the address impressed to the examined semiconductor

device, The timing selection circuitry which sets up the generating timing of the strobe pulse corresponding to this phase number whenever the phase number memorized by G and this memory is read, The strobe generating circuit which generates the strobe pulse impressed to the above-mentioned data reading circuit according to the timing setting value set as H and this timing selection circuitry, and the semiconductor device testing device characterized by constituting "Be alike."

[Claim 7] A and the data reading circuit which reads the data which an examined semiconductor device outputs according to the impression timing of a strobe pulse, Two or more signal reading circuits prepared in order to measure the generating timing of the reference clock which B and the above-mentioned examined semiconductor device output, C and a polyphase pulse generating means to impress the strobe pulse which consists of polyphase pulses by which small [every] phase contrast was given to each of two or more of these signal reading circuits, Two or more comparison test means to compare with expected value the result which each of D and two or more above-mentioned signal reading circuits read, E and a conversion means to change the judgment result of two or more of these comparison test means into the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock, The memory memorized to the address corresponding to the address showing the chronological-order foreword of a test pattern which impressed the phase number which F and this conversion means changed to the examined semiconductor device, The timing selection circuitry which sets up the generating timing of the strobe pulse corresponding to this phase number whenever the phase number memorized by G and this memory is read, The strobe generating circuit which generates the strobe pulse impressed to the above-mentioned data reading circuit according to the timing setting value set as H and this timing selection circuitry, and the semiconductor device testing device characterized by constituting "Be alike."

[Claim 8] It sets they to be [any of a semiconductor device testing device according to claim 6 or 7], and, for the above-mentioned polyphase pulse generating means, a time delay is the semiconductor device testing device characterized by generating the polyphase pulse to which it was constituted by two or more different delay elements, the pulse was impressed to the delay element of these plurality, and small [every] phase contrast was given every only.

[Claim 9] It is the semiconductor device testing device characterized by having set they being [any of a semiconductor device testing device according to claim 6 or 7], and for the polyphase pulse generating means having carried out cascade connection of two or more delay elements with the same time delay, and considering as the configuration which acquires a polyphase pulse from each node of two or more of these delay elements that carried out cascade connection.

[Claim 10] It sets they to be [any of a semiconductor device testing device according to claim 6 or 7]. Two or more above-mentioned comparison test means output the comparison test result to the comparison test means by which a time delay is long, next sequentially from a side with the short time delay of the strobe pulse which consists of above-mentioned polyphase pulses. Each comparison test means makes the judgment result to confirm output only from the comparison test means which detected the comparison test result and inequality of each preceding paragraph. The semiconductor device testing device characterized by considering as the configuration which changes the output bit position of this judgment result to confirm into the phase number of the strobe pulse which detected the changing point of the above-mentioned reference clock.

[Translation done.]

* NOTICES *

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The block diagram showing one example of the semiconductor device testing device which operates using the semiconductor device test method by this invention.

[Drawing 2] The block diagram for explaining the outline of a common semiconductor device testing device.

[Drawing 3] The timing chart for explaining actuation of the important section of the semiconductor device testing device by this invention shown in drawing 1 .

[Drawing 4] The same timing chart for explaining other examples of a timing chart shown in drawing 3 .

[Drawing 5] The block diagram for explaining an example of the configuration of the comparison test means used for the semiconductor device testing device by this invention shown in drawing 1 .

[Drawing 6] Drawing for explaining actuation of the comparison test means shown in drawing 5 .

[Drawing 7] The block diagram for explaining the configuration of the timing selection circuitry used for the semiconductor device testing device by this invention shown in drawing 1 .

[Drawing 8] The block diagram showing the deformation example of the semiconductor device testing device by this invention shown in drawing 1 .

[Drawing 9] The block diagram showing the deformation example of further others of the semiconductor device testing device by this invention.

[Drawing 10] The timing chart for explaining the description of the semiconductor device which it is going to examine by this invention.

[Drawing 11] The timing chart for explaining the trouble which the semiconductor device explained by drawing 10 has.

[Drawing 12] The block diagram for explaining a signal reading circuit to be the level comparator with which the semiconductor device testing device is equipped.

[Drawing 13] The timing chart for explaining actuation of the level comparator and signal reading circuit which were shown in drawing 12 .

[Description of Notations]

DQS Reference clock

DUT Examined semiconductor device

10 Level Comparator

CP1, CP2 Electrical-potential-difference comparator

11 Signal Reading Circuit

TC1 -- TC5 Signal reading circuit

PF1 -- PF5 Comparison test means

12 Logic Comparator

P1 -- P6 Polyphase pulse

30 Polyphase Pulse Generator

31 Conversion Means

32 Memory

33 Timing Selection Circuitry

34 Strobe Generating Circuit

35 Address Translation Circuit

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[Drawing 1]

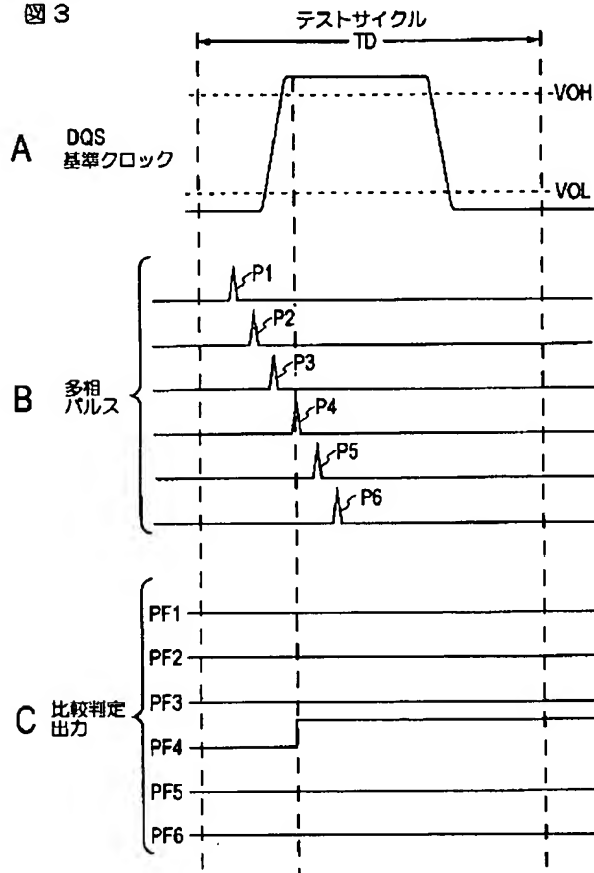


[Drawing 2]



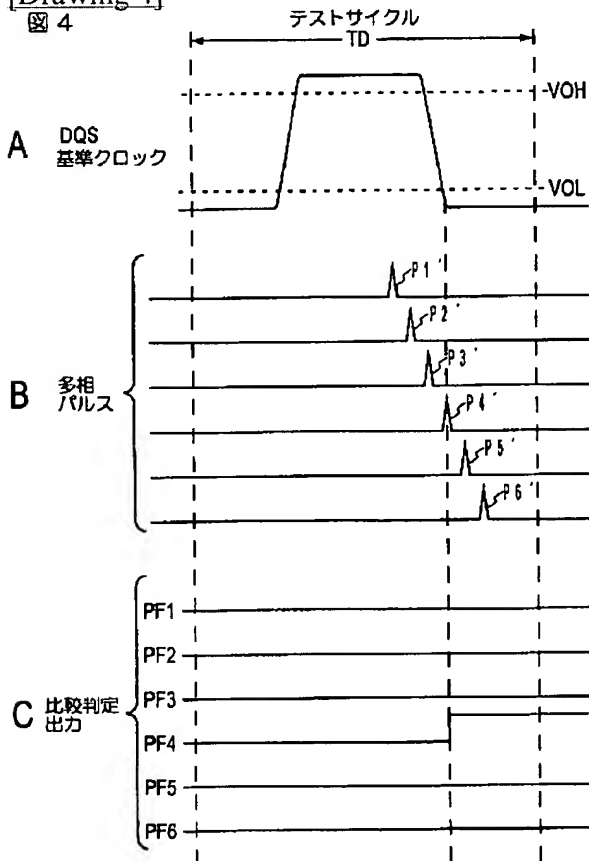
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図 3



[Drawing 4]

図 4



[Drawing 5]

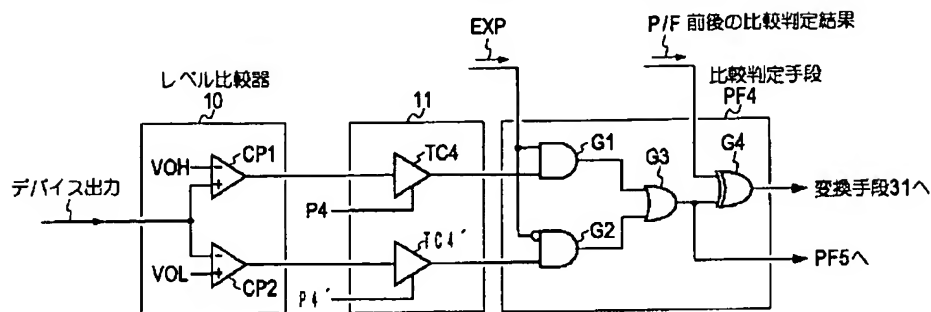


図 5

[Drawing 6]

バスフェイル

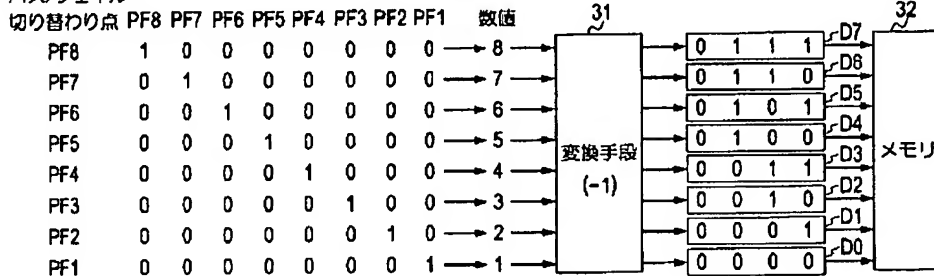
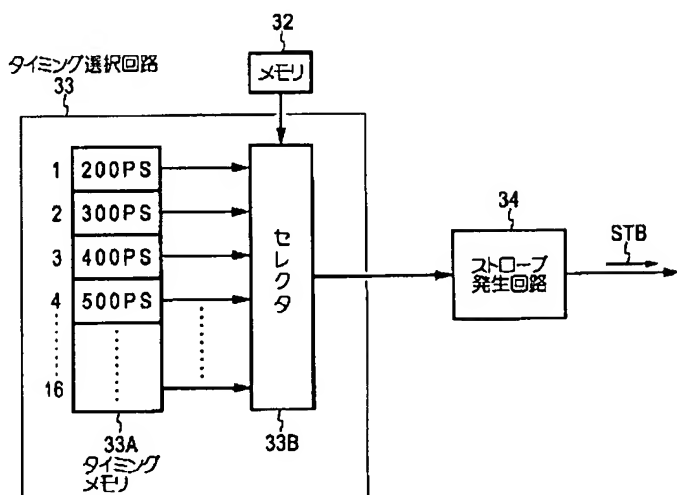


図 6

[Drawing 7]

図 7



[Drawing 10]

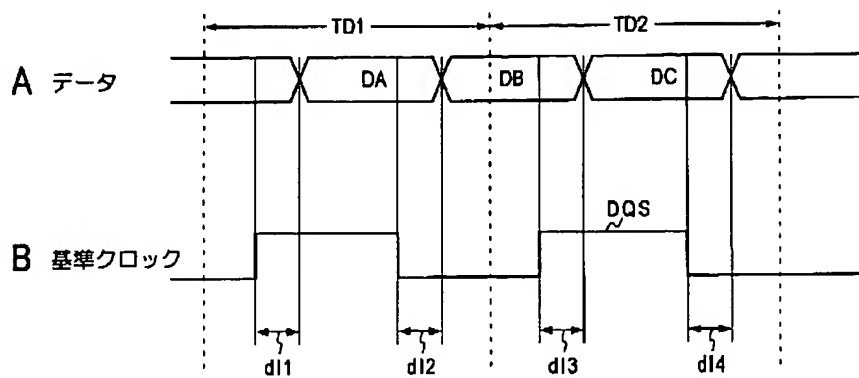


図 10

[Drawing 8]

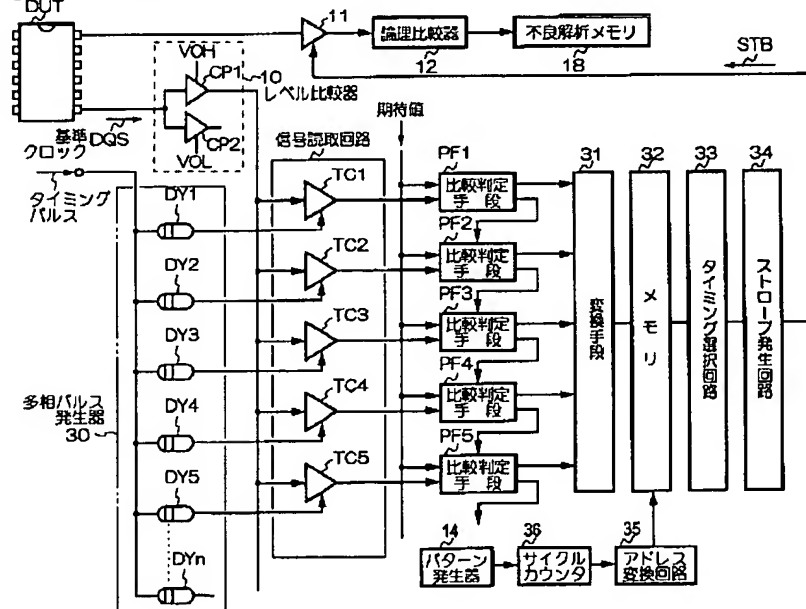


図 8

[Drawing 9]

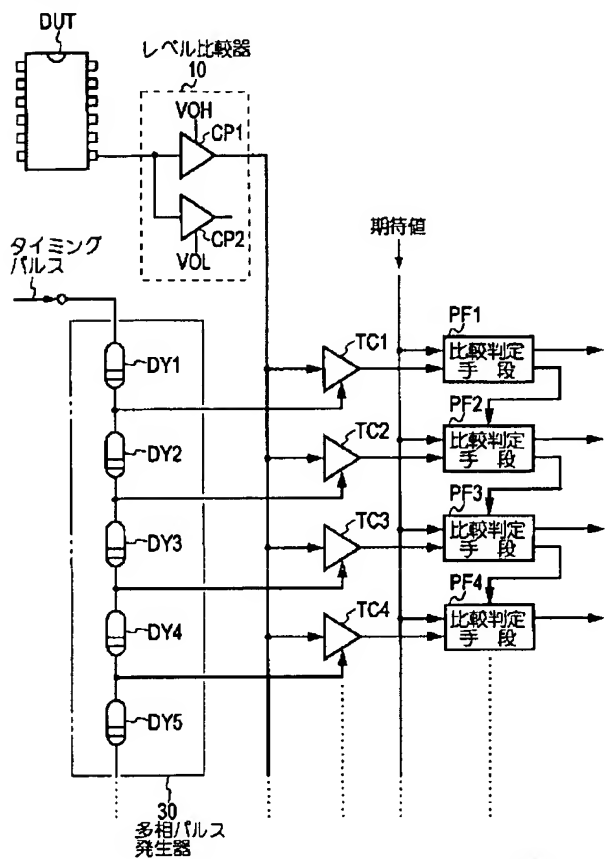
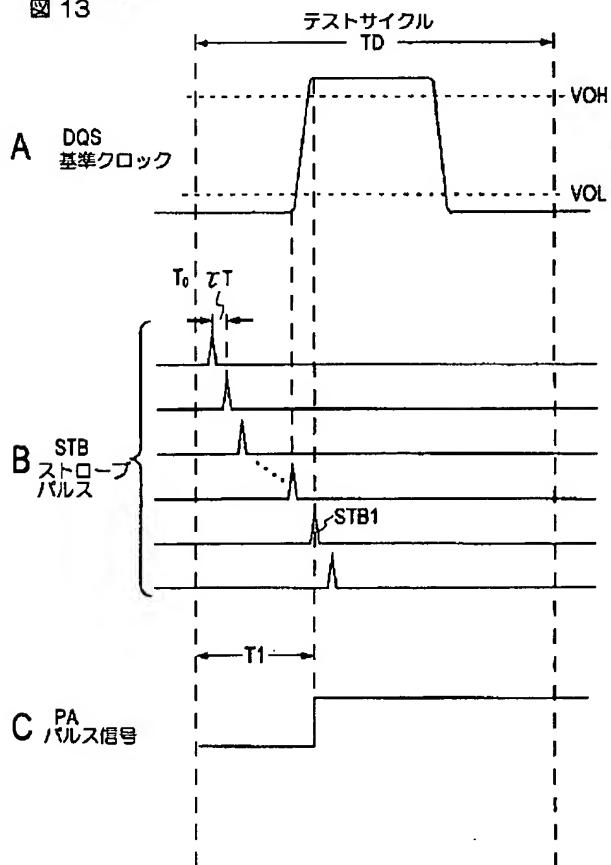


図 9

[Drawing 13]

図 13



[Drawing 11]

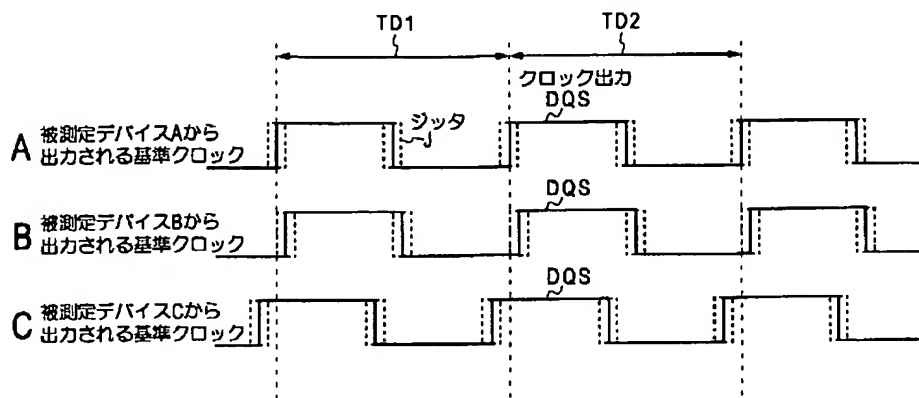


図 11

[Drawing 12]

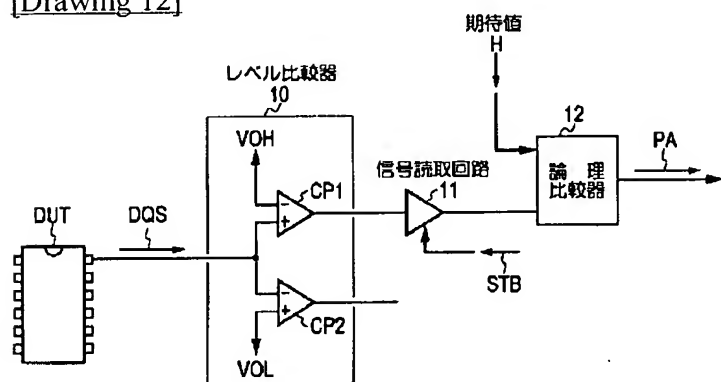


図 12

[Translation done.]